

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Currently amended) A switch comprising:

a plurality of ports ~~for configured to exchange exchanging data;~~ and

a shared[[-]] memory ~~for configured to enable enabling the exchange of data for a selected one of a plurality of word-widths between first and second ones of said- the plurality of ports, wherein the shared memory is further configured to enable the selected word-width to be programmatically provided to the shared memory, and said- wherein the shared[[-]] memory comprising includes:~~

an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width that differs from at least the selected word-width;

circuitry ~~for configured to write writing selected data presented at said- the first one of said- the plurality of ports into a selected row in said- the array as a word of the predetermined word-width during a first time period and for to read the reading said selected data as a word of the predetermined word-width from said- the selected row during a second time period, and for to output the read data at the said- second one of said- the plurality of ports, wherein the circuitry is further configured to bridge the selected word-width and the pre-determined word-width.~~

2. (Currently amended) The switch of claim 1, ~~and further comprising a buffer associated with each a selected one of the first and second ports for and configured to cooperate with the shared memory to bridge the selected word-width and the pre-determined word-width converting words of data from an initial bit-width to said predetermined bit width.~~

3. (Currently amended) The switch of claim 1, ~~wherein said the predetermined bit word-width is equal to a bit word-width of certain bit-width and associated overhead.~~

4. (Currently amended) The switch of claim 2, wherein ~~said the~~ initial bit selected word- width is 48 bits and ~~said the~~ predetermined bit word- width is 384 bits.

5. (Currently amended) The switch of claim 1, wherein ~~said the~~ circuitry for reading and writing comprises an available address table ~~for~~ configured to store storing write addresses available for selection and use in writing to selected rows ~~said in the~~ array.

6. (Currently amended) The switch of claim 5, wherein ~~said the~~ circuitry for reading and writing further comprises a used address table ~~for~~ configured to store storing addresses already used for writing data to selected rows in ~~said the~~ array.

7. (Currently amended) The switch of claim 1, wherein ~~said the~~ array comprises an array of random access memory cells of the read/write classification.

8. (Currently Amended) A switch [[,]] comprising:

a plurality of ports configured to exchange data with external devices, wherein the data has a selected one of a plurality of word-widths;

a memory including a plurality of banks, each bank having an array of memory cells arranged as a plurality of rows, wherein each row comprises ~~y number~~ a plurality of memory cells forming a predetermined word-width that differs from at least the selected word-width, and wherein the memory further comprises circuitry configured to select one of the plurality of rows in response to a received address;

a buffer associated with one of the plurality of ports and configured to assemble ~~a stream of data words~~ the data with the selected word-width, as received by the one of the ~~plurlaity plurality~~ plurality of ports, ~~into a single word having a predetermined width,~~ wherein the ~~predetermined width includes x number of bits,~~ and ~~wherein y divided by x results in an integer greater than one~~ wherein the buffer is further configured to cooperate with the circuitry of the memory to bridge the selected word-width and the pre-determined word-width;

a plurality of available address tables, each available address table including a queue of addresses available for writing data to a corresponding one of the banks; and

a plurality of used address tables, each used address table including a queue of addresses for reading from a corresponding one of the banks;

wherein the switch is configured to enable the selected word-width to be programmatically provided to the switch.

9. (Currently amended) The switch of claim 8, wherein the ~~data-stream of data words~~ comprises eight forty-eight bit words of ATM data.

10. (Previously presented) The switch of claim 8, wherein each of the plurality of available address tables comprises a first-in-first-out memory.

11. (Previously presented) The switch of claim 8, wherein each of the plurality of used address tables comprises a random access memory configured to perform read and write operations.

12. (Currently amended) The switch of claim 8, wherein each of the banks ~~is~~are randomly accessible.

13. (Currently amended) The switch of claim 8, wherein each of the banks ~~is~~are designated to store data from corresponding ones of the plurality of ports.

14. (Currently amended) The switch of claim 8, wherein each of the banks ~~is~~are designated to store data from more than one of the plurality of ports.

15. (Previously presented) The switch of claim 8, wherein the memory comprises i number of banks and the switch comprises j number of ports, where $i < j$.

16. (Currently amended) A digital information system comprising:

first and second resources operable to exchange data in a selected one of a plurality of digital formats, wherein data of the selected digital format has a data size equal to a word-width; and

a digital switch ~~comprising~~ including:

first and second ports ~~for configured to selectively coupling~~ couple the said first and second resources; and

a shared memory ~~for configured to enable~~ enabling the exchange of data between ~~said the~~ first and second ports ~~as words of a predetermined word-width, said wherein the shared~~ comprising comprises:

an array of memory cells arranged as a plurality of rows and a single column having a width equal to ~~said a~~ a predetermined word-width that differs from the word-width for the data size of the data of the selected digital format; and

circuitry ~~for configured to write~~ writing a selected data word presented at ~~said the~~ first one of ~~said the~~ plurality of ports to a selected row in ~~said the~~ array during a first time period, ~~and for reading said to read the~~ selected data word from ~~said the~~ selected row during a second time period, and to output the read data at said the second one of said the plurality of ports, wherein the circuitry is further configured to bridge the word-width for the data size of the data of the selected digital format and the pre-determined word-width;

wherein the digital switch is configured to enable the word-width for the data size of the data of the selected digital format to be programmatically provided to the digital switch.

17. (Currently amended) The system of claim 16, ~~wherein data are exchanged through said ports as streams of data words of an initial word-width and said switch further comprises buffers for converting data words between said initial word-width and said predetermined word-width~~ further comprising a buffer associated with each of the first and second ports, and configured to cooperate with the shared memory to bridge the word-width for the data

size of the data of the selected digital format and the pre-determined word-width.

18. (Currently amended) The system of claim 16, wherein ~~said~~ the selected digital format comprises ~~[[as]]~~ an Asynchronous Transfer Mode digital data format.

19. (Currently amended) The system of claim 18, wherein ~~said~~ the predetermined word-width equals a bit-width of a user data portion of an asynchronous transfer mode information packet.

20. (Currently amended) The system of claim 16, wherein ~~said~~ the first and second resources are selected from the group ~~comprising~~ consisting of digital telephones, digital facsimile machines, digital data networks, home networks, digital private branch exchanges, workstations, and video teleconferencing equipment.

21. (Currently amended) The system of claim 16, wherein the shared memory data interface is selected from the group consisting of DDR (double data rate), QDR (quad data rate), Rambus.TM., and programmable ~~bit~~ burst ~~bit~~ length ~~memories~~ interfaces.

22-32 (Canceled)